CLAIMS

What is claimed is:

1. A method of providing defect data for programmable logic devices (PLDs), the PLDs each having a unique identifier, the method comprising:

testing a plurality of the PLDs and selecting therefrom a plurality of defective PLDs containing localized defects;

recording defect data for each defective PLD, the defect data comprising the unique identifier for each defective PLD and location information for each detected defect within the defective PLD;

maintaining a database of the defect data;

receiving a first identifier from a user; and

providing to the user location information from the database corresponding to the first identifier.

2. The method of Claim 1, wherein:

receiving the first identifier from the user is accomplished via a data communications link; and

providing to the user location information from the database corresponding to the first identifier is accomplished via the data communications link.

3. The method of Claim 1, wherein the location information comprises identification information for at least a portion of one or more logic blocks affected by the localized defects.

4. The method of Claim 1, wherein the location information comprises coordinates specifying the location of each localized defect.

5. The method of Claim 1, further comprising:

implementing a user design in a first defective PLD having the first identifier.

6. The method of Claim 1, further comprising:

receiving a second identifier from a user; and

providing to the user location information from the database corresponding to the second identifier.

7. The method of Claim 1, wherein the PLD is a field programmable gate array (FPGA).

8. The method of Claim 7, wherein maintaining the database of the defect data comprises:

generating a defect map for each defective PLD; and

generating a constraints file for each defective PLD based on a corresponding defect map,

and wherein providing to the user location information from the database comprises providing a constraints file corresponding to the first identifier.

9. A method of implementing a user design in a defective programmable logic device (PLD), the PLD having a unique identifier, the method comprising:

creating the user design;

providing to a PLD provider a first identifier corresponding to a first defective PLD;

obtaining from the PLD provider, based on the first identifier, defect data comprising first location information for first localized defects in the first defective PLD; and

implementing the user design in the first defective PLD while using the first location information to avoid utilizing first PLD resources affected by the first localized defects.

10. The method of Claim 9, wherein:

providing to the PLD provider the first identifier is accomplished via a data communications link; and

obtaining from the PLD provider the defect data is accomplished via the data communications link.

11. The method of Claim 9, wherein the first location information comprises identification information for at least a portion of one or more logic blocks in the first defective PLD affected by the first localized defects.

12. The method of Claim 9, wherein the first location information comprises coordinates specifying a location of each first localized defect.

13. The method of Claim 9, further comprising implementing the user design in a fully functional PLD to produce a first implemented design, and wherein:

implementing the user design in the first defective PLD comprises performing an incremental compilation with respect to the first implemented design.

14. The method of Claim 9, further comprising:

providing to the PLD provider a second identifier corresponding to a second defective PLD;

obtaining from the PLD provider, based on the second identifier, defect data comprising second location information for second localized defects in the second defective PLD; and

implementing the user design in the second defective PLD while using the second location information to avoid utilizing second PLD resources affected by the second localized defects.

15. The method of Claim 14, wherein:

implementing the user design in the first defective PLD produces a first implemented design; and

implementing the user design in the second defective PLD comprises performing an incremental compilation with respect to the first implemented design.

16. The method of Claim 9, wherein the PLD is a field programmable gate array (FPGA).

17. The method of Claim 16, wherein the defect data comprises a constraints file for the first defective PLD.

18. The method of Claim 16, wherein:

the PLD is an FPGA programmable from a PROM; and

implementing the user design in the first defective PLD is performed by PROM programming software.

19. The method of Claim 16, wherein implementing the user design in the first defective PLD comprises:

placing and routing the user design in the first defective PLD while using the location information to avoid using defective portions of the first defective PLD; and

generating an FPGA bitstream implementing the user design in the first defective PLD.

20. A method of providing custom design files for programmable logic devices (PLDs), the PLDs each having a unique identifier, the method comprising:

testing a plurality of the PLDs and selecting therefrom a plurality of defective PLDs containing localized defects;

recording defect data for each defective PLD, the defect data comprising the unique identifier for each defective PLD and location information for each detected defect within the defective PLD;

maintaining a database of the defect data;

receiving a first design file from a user, the design file being an implementation targeted towards a fully functional version of the defective PLDs;

receiving a first identifier from the user uniquely identifying a first defective PLD of the plurality of defective PLDs;

retrieving from the database, based on the first identifier, first location information for the first defective PLD;

performing an incremental compilation with respect to the first design file while using the first location information to avoid the localized defects of the first defective PLD, the incremental compilation generating a second design file; and

providing the second design file to the user.

21. The method of Claim 20, wherein:

receiving the first identifier from the user is accomplished via a data communications link; and

providing the second design file to the user is accomplished via the data communications link.

22. The method of Claim 20, further comprising:

receiving a second identifier from the user uniquely identifying a second defective PLD of the plurality of defective PLDs;

retrieving from the database, based on the second identifier, second location information for the second defective PLD;

performing a second incremental compilation with respect to the first design file while using the second location information to avoid the localized defects of the second defective PLD, the second incremental compilation generating a third design file; and

providing the third design file to the user.

23. The method of Claim 20, wherein the PLD is a field programmable gate array (FPGA).

24. The method of Claim 23, wherein maintaining the database of the defect data comprises:

generating a defect map for each defective PLD; and

generating a constraints file for each defective PLD based on a corresponding defect map,

and wherein performing an incremental compilation with respect to the first design file comprises using the constraints file corresponding to the first defective PLD.

25. A method of providing defect data for programmable logic devices (PLDs), the PLDs each having a unique identifier, the method comprising:

testing a plurality of the PLDs for device-specific information;

recording data for each tested PLD, the data comprising the unique identifier and the device-specific information for each PLD;

maintaining a database of the recorded data;

receiving a first identifier from a user; and

providing to the user the device-specific information from the database corresponding to the first identifier.

26. The method of Claim 25, wherein:

receiving the first identifier from the user is accomplished via a data communications link; and

providing to the user the device-specific information from the database corresponding to the first identifier is accomplished via the data communications link.

27. The method of Claim 25, further comprising:

implementing a user design in a first PLD having the first identifier.

28. The method of Claim 25, further comprising:

receiving a second identifier from a user; and

providing to the user the device-specific information from the database corresponding to the second identifier.

29. The method of Claim 25, wherein the PLD is a field programmable gate array (FPGA).

30. The method of Claim 25, wherein the device-specific information comprises information relating to the speed of various sub-components of the PLD.

31. The method of Claim 25, wherein the device-specific information comprises configuration information for the PLD.

32. The method of Claim 25, wherein the device-specific information comprises information relating to defects in the PLD.

33. A method of implementing a user design in a programmable logic device (PLD), the PLD having a unique identifier, the method comprising:

creating the user design;

providing to a PLD provider a first identifier corresponding to a first PLD;

obtaining from the PLD provider, based on the first identifier, device-specific information for the first PLD; and

implementing the user design in the first PLD using the device specific information for the first PLD.

34. The method of Claim 33, wherein:

providing to the PLD provider the first identifier is accomplished via a data communications link; and

obtaining from the PLD provider the device-specific information is accomplished via the data communications link.

35. The method of Claim 33, further comprising:

providing to a PLD provider a second identifier corresponding to a second PLD;

obtaining from the PLD provider, based on the second identifier, device-specific information for the second PLD; and

implementing the user design in the second PLD using the device specific information for the second PLD.

36. The method of Claim 33, wherein the PLD is a field programmable gate array (FPGA).

37. The method of Claim 33, wherein the device-specific information comprises information relating to the speed of various sub-components of the PLD.

38. The method of Claim 33, wherein the device-specific information comprises configuration information for the PLD.

39. The method of Claim 33, wherein the device-specific information comprises information relating to defects in the PLD.